

09395565-062901

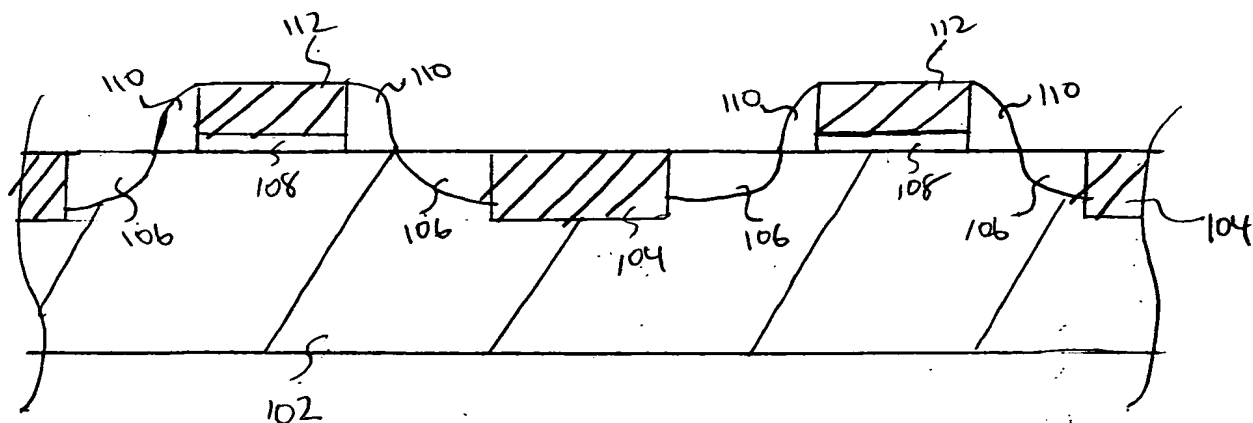


FIG. 1A

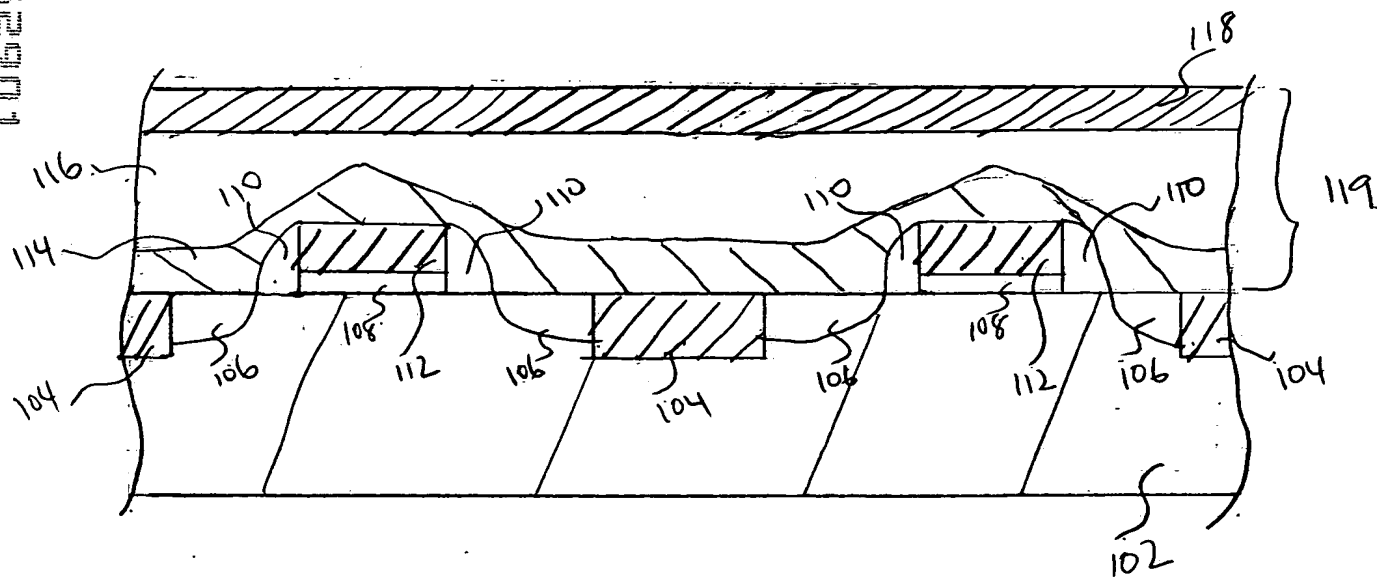


FIG. 1B

This cross-sectional view shows a semiconductor device with a common source region 102 at the bottom. A gate stack 104 is formed on the source region, with a gate dielectric 106 and a gate conductive layer 110. The gate stack is divided into five gates 112, 118, 120, 122, and 121. A channel region 114 is formed in the substrate 102 between the gates. A source region 116 is formed in the substrate 102 on the left side of the first gate 112. A drain region 118 is formed in the substrate 102 on the right side of the last gate 121. A top layer 120 is formed on the channel region 114 and the source region 116. A top layer 122 is formed on the drain region 118. A top layer 121 is formed on the top layer 120. A top layer 119 is formed on the top layer 121.

FIG 1C

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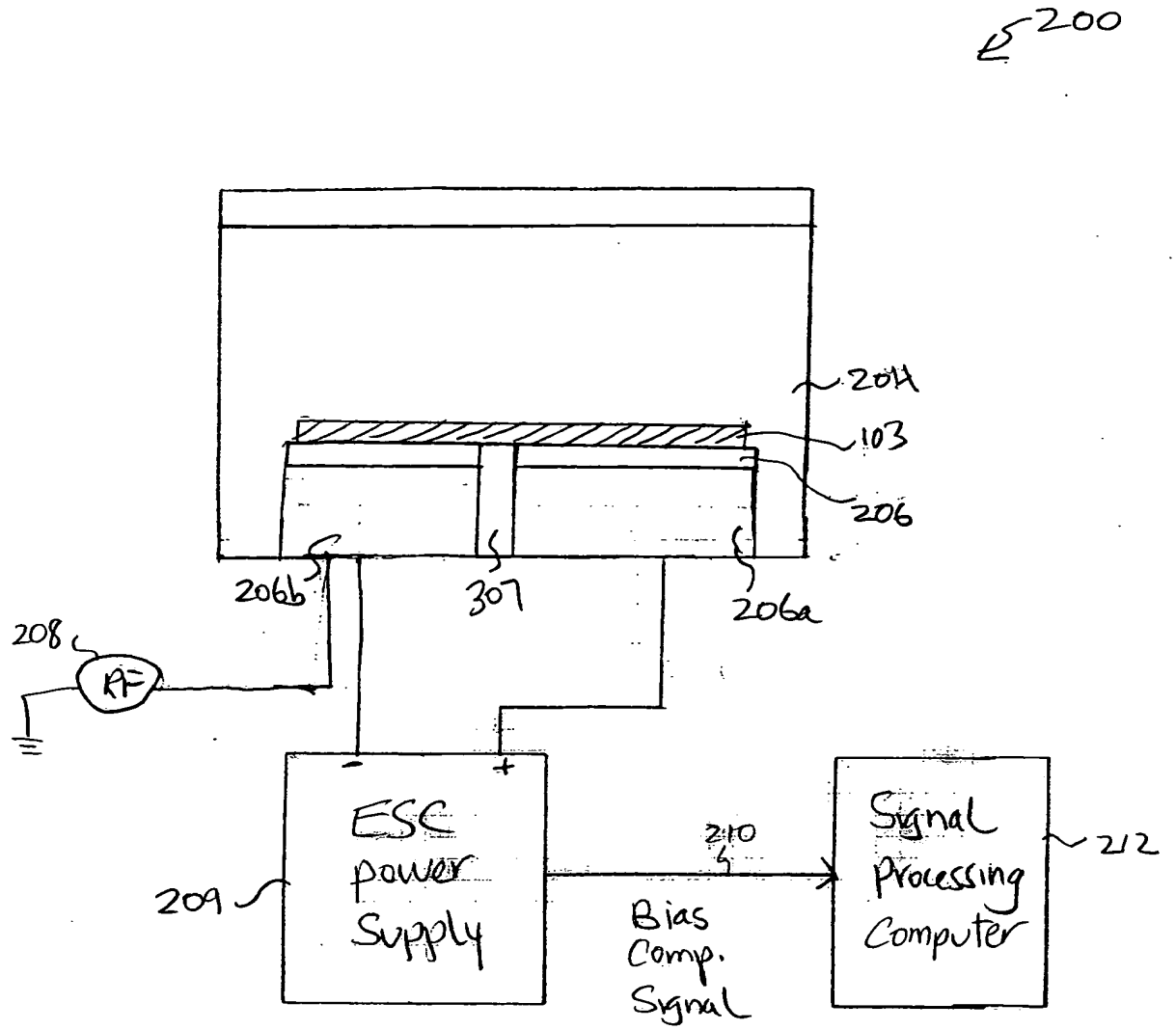


FIG. 2

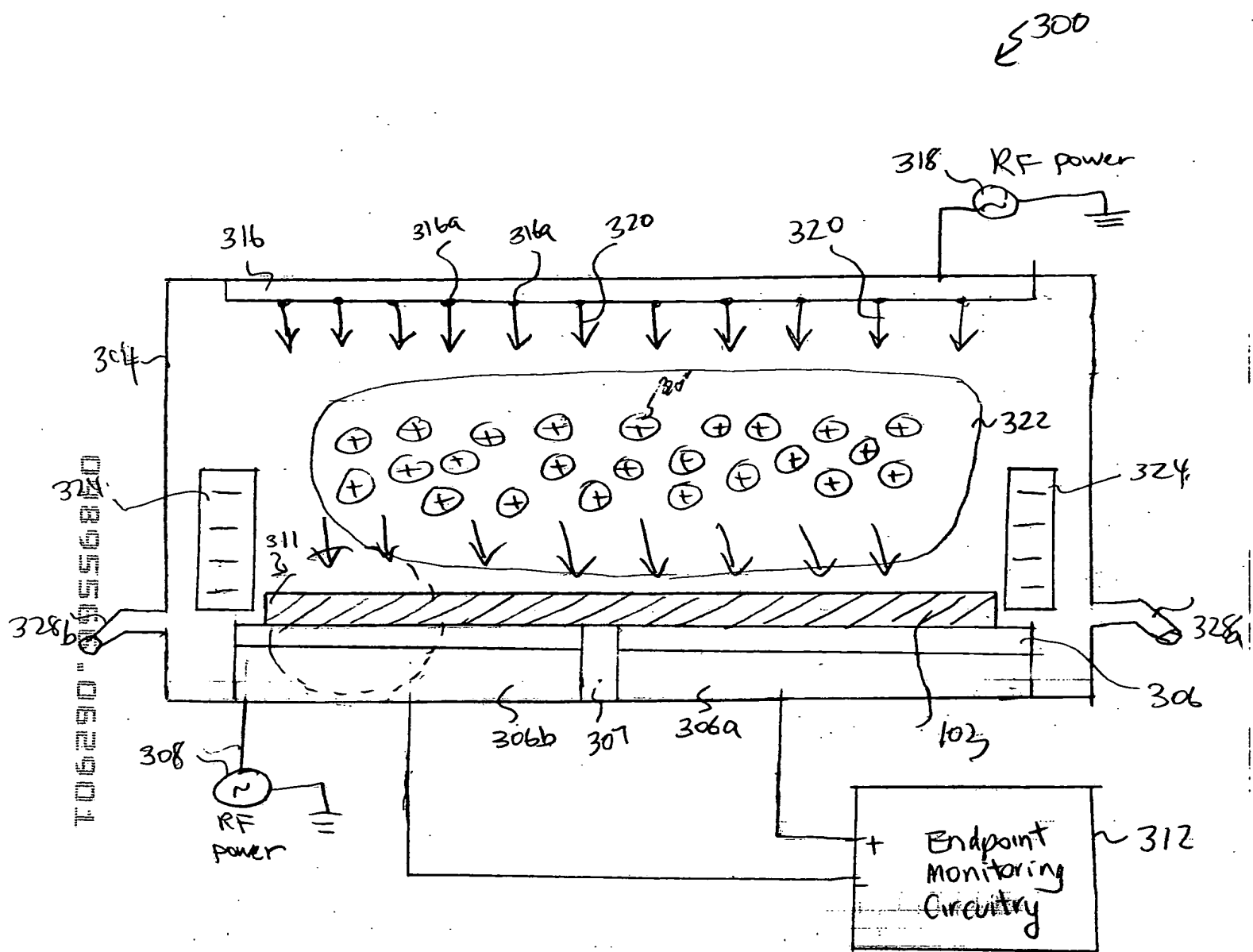


FIG. 3A

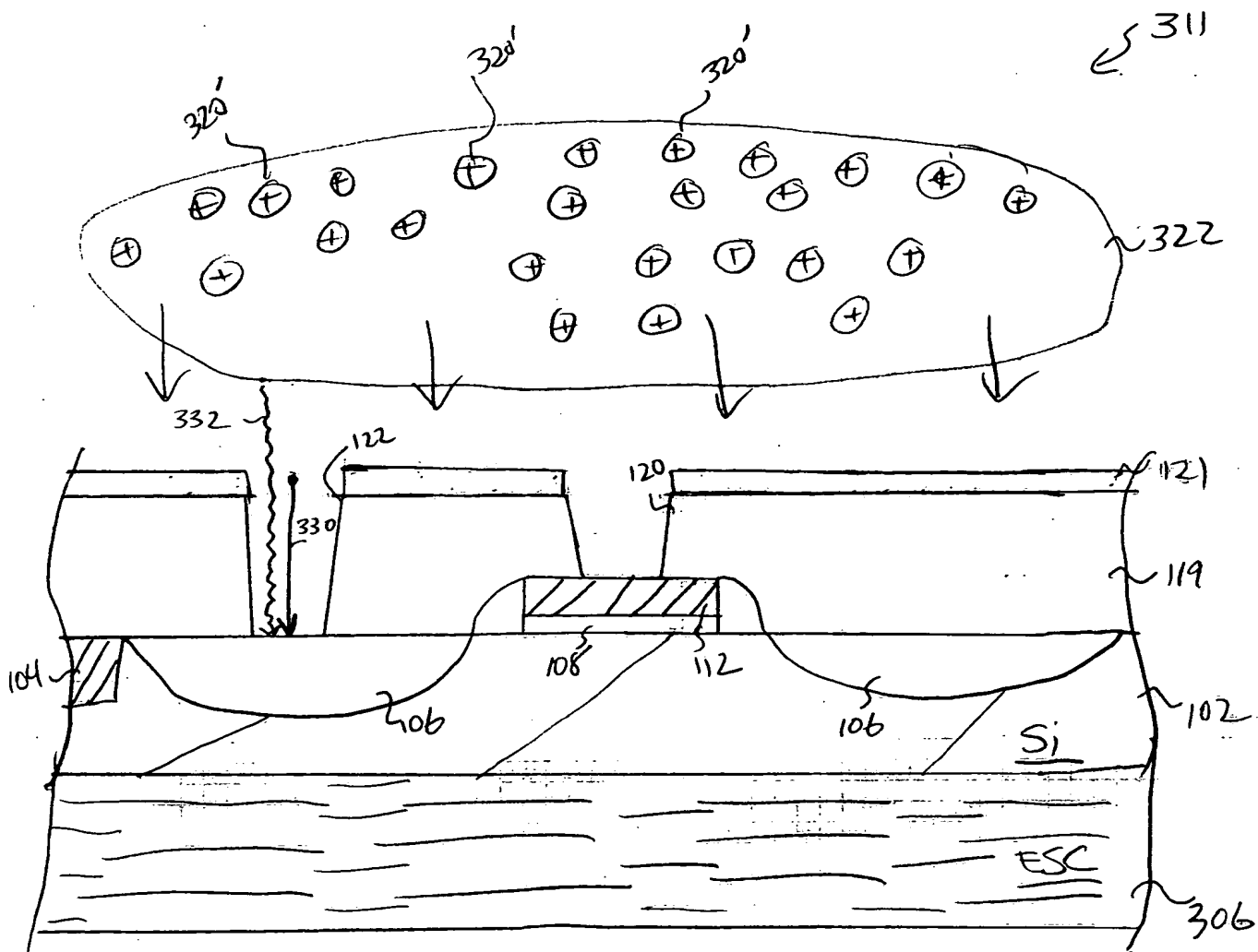


FIG. 3B

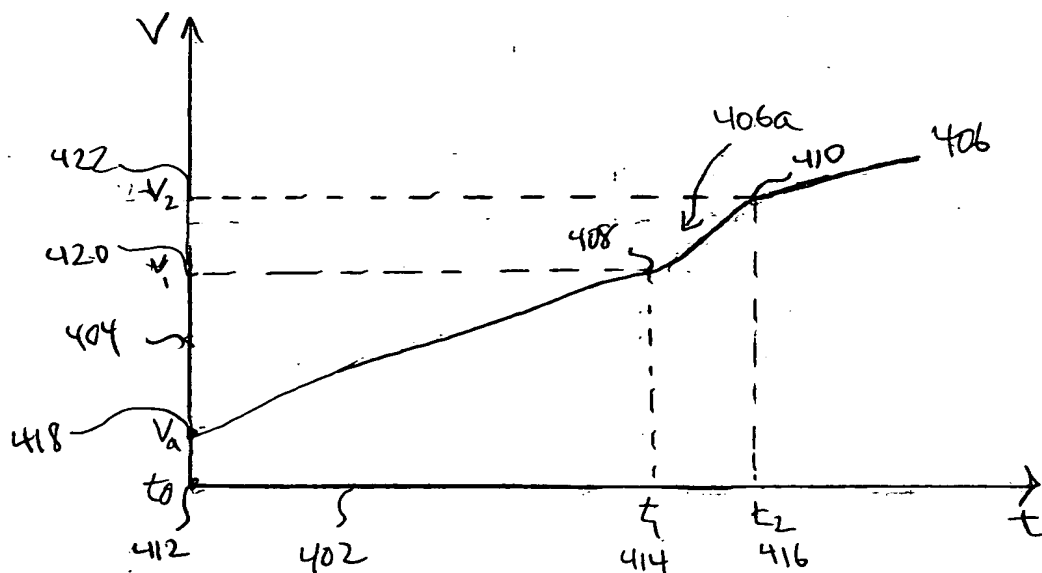
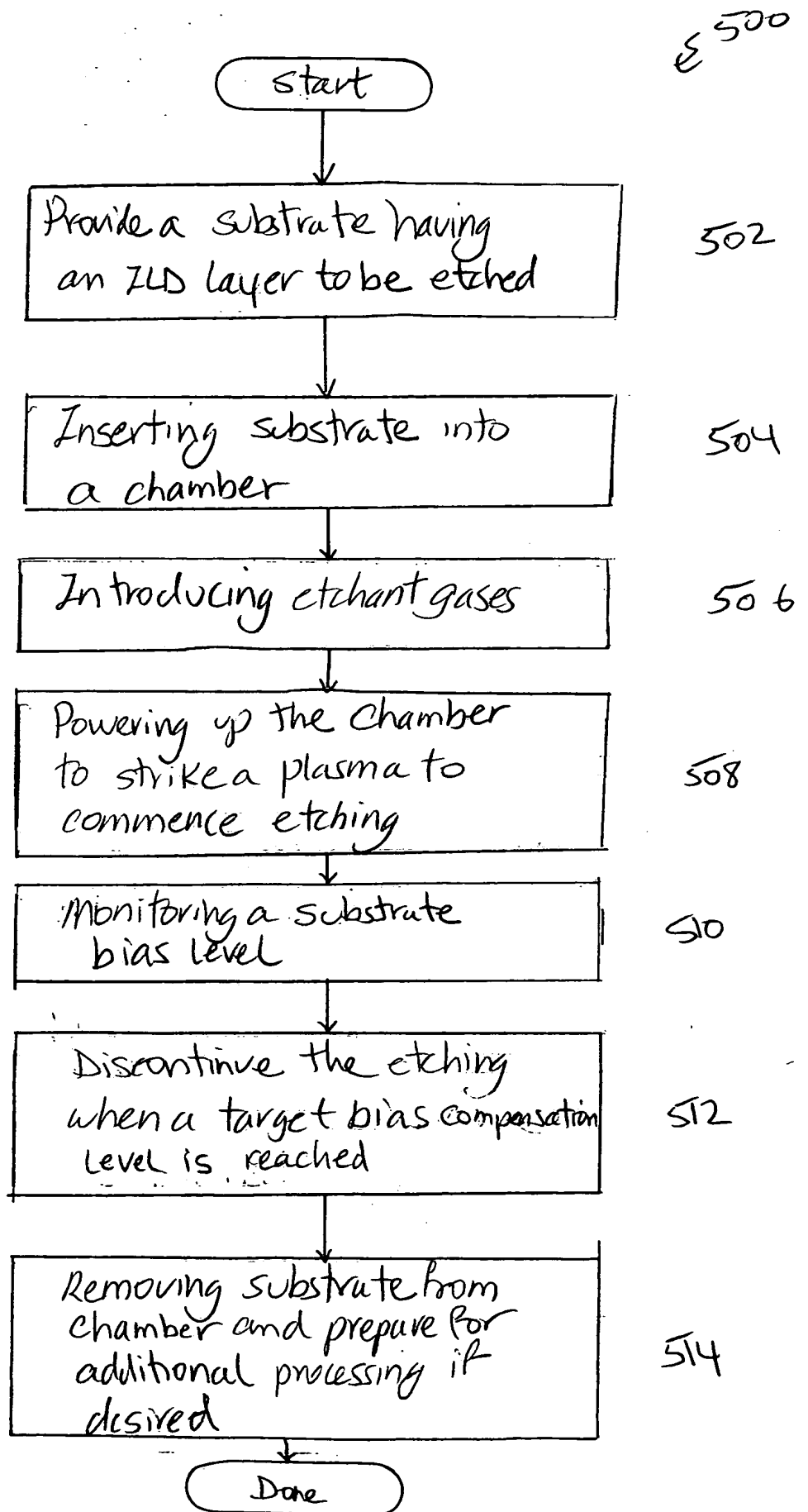


FIG. 4

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FIG. 5A



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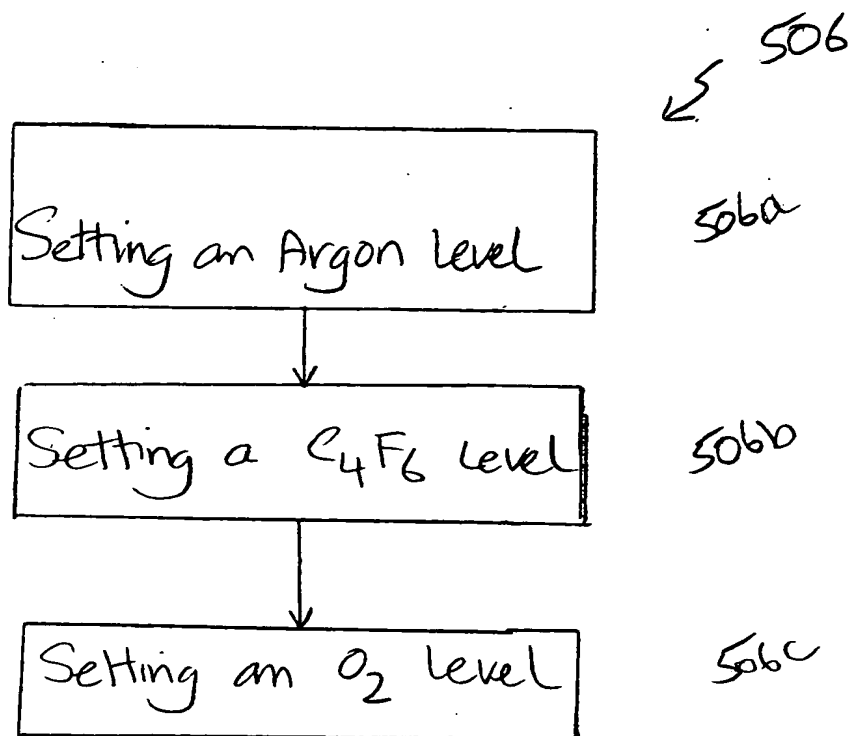


FIG. 5B

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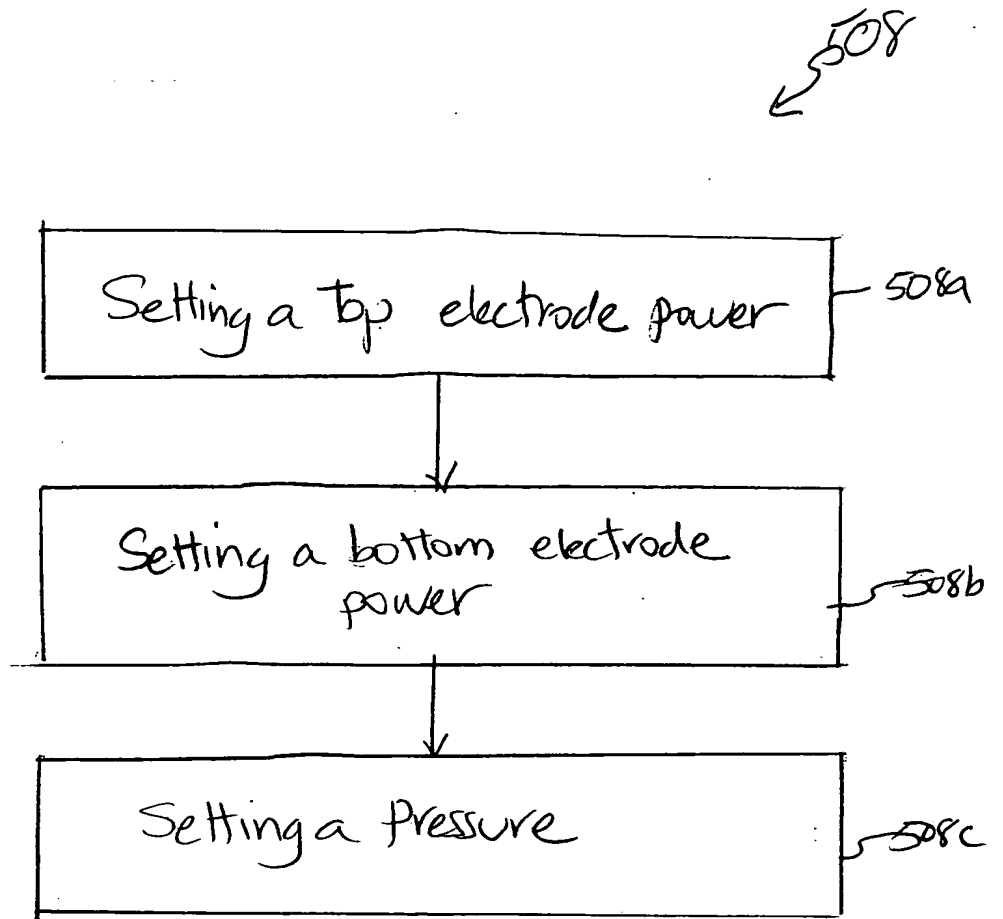


FIG. 5C